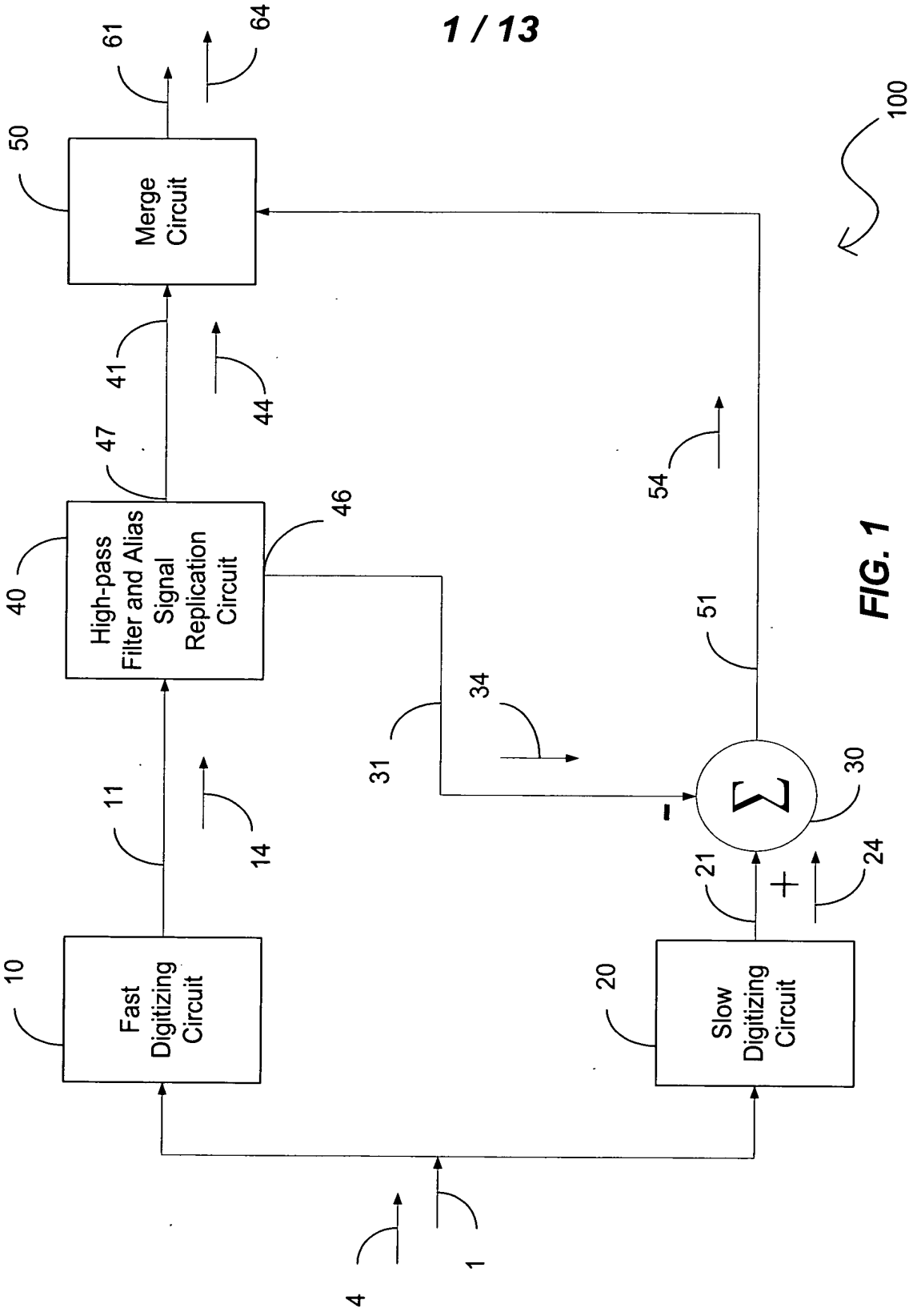
100
Merge Circuit
50
61
64
41
44
High-pass Filter and Alias Signal Replication Circuit
40
47
46
54
51
34
31
30
Σ
-
+
21
24
11
14
Fast Digitizing Circuit
10
Slow Digitizing Circuit
20
4
1

FIG. 1

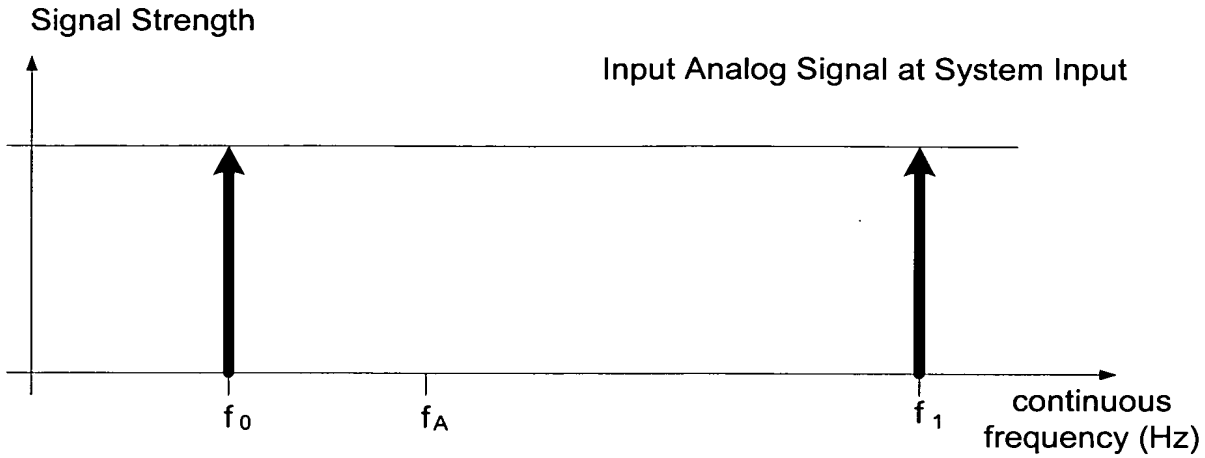

FIG. 2A

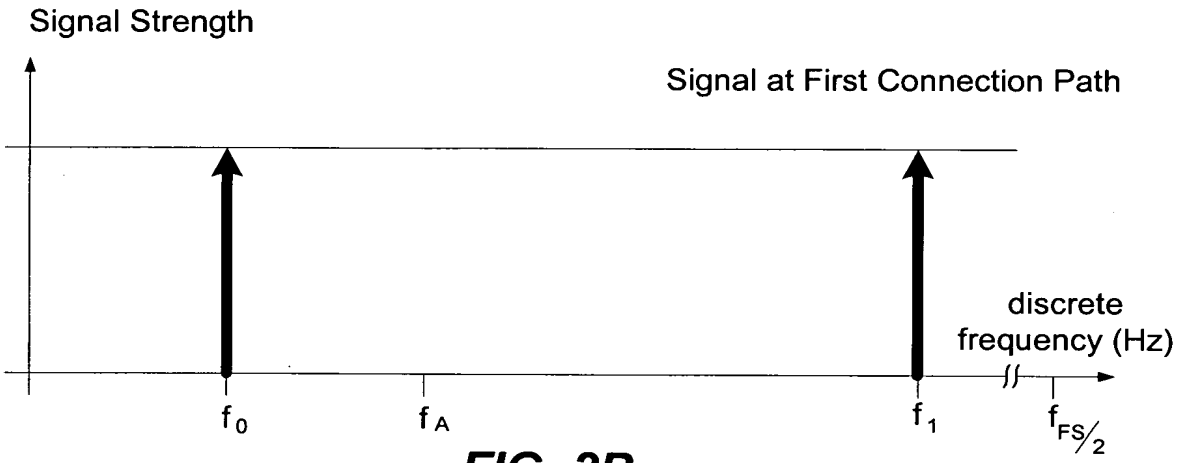

FIG. 2B

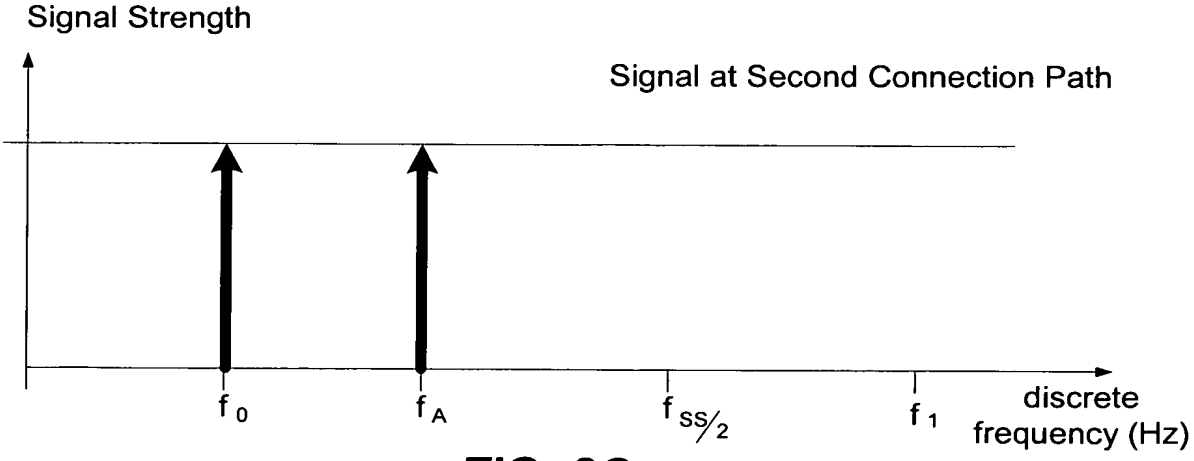

FIG. 2C

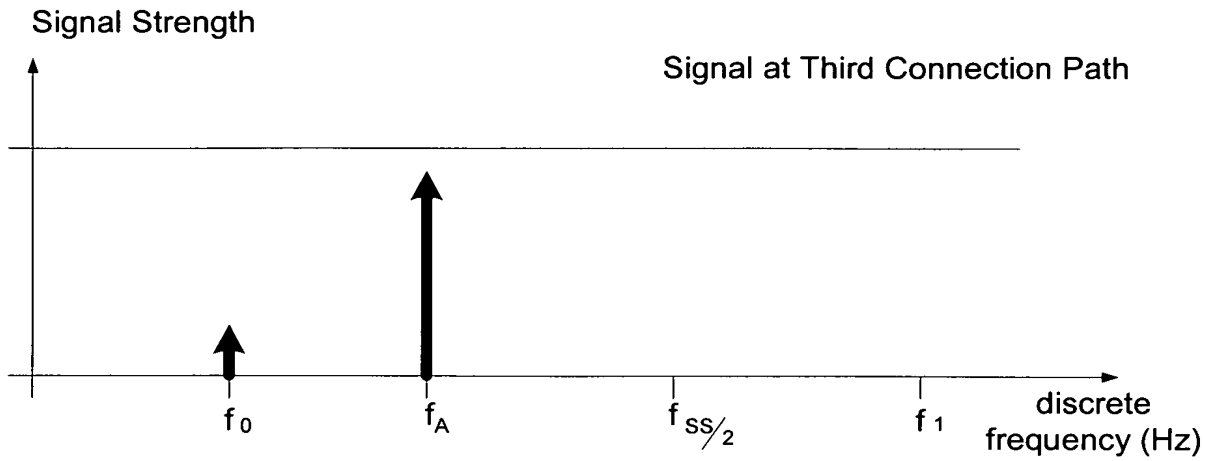

FIG. 2D

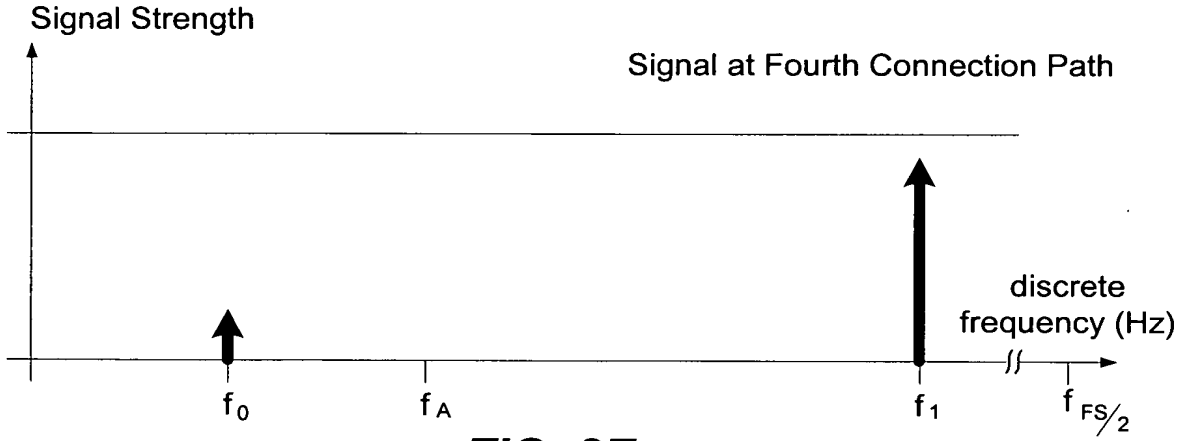

FIG. 2E

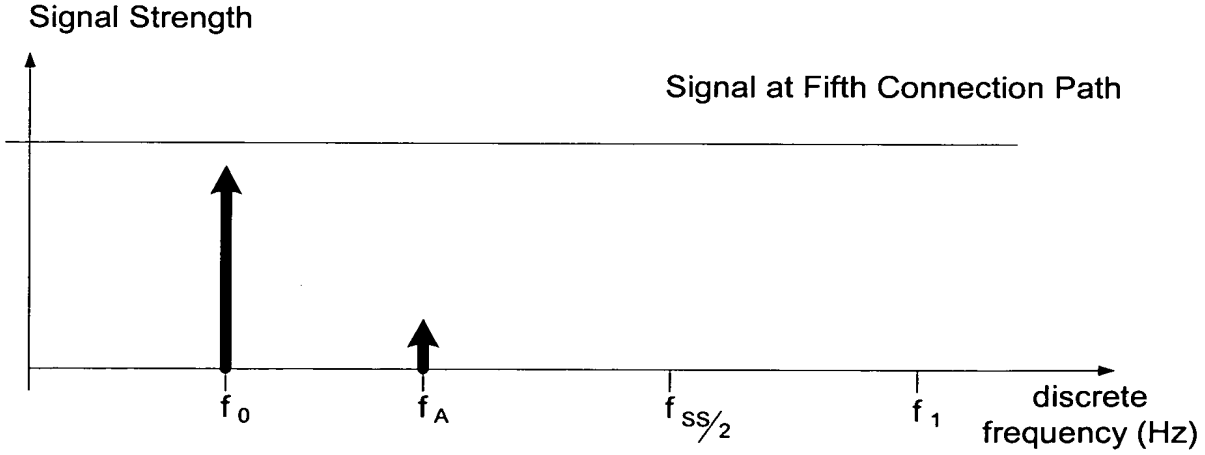

FIG. 2F

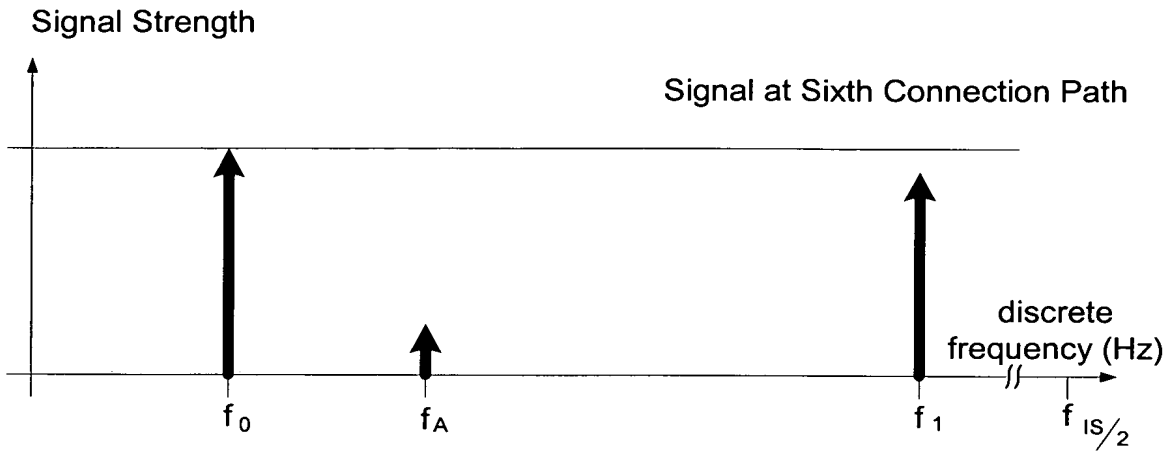
Signal Strength
Signal at Sixth Connection Path
discrete
frequency (Hz)
f 0
fA
f 1
f IS/2

FIG. 2G

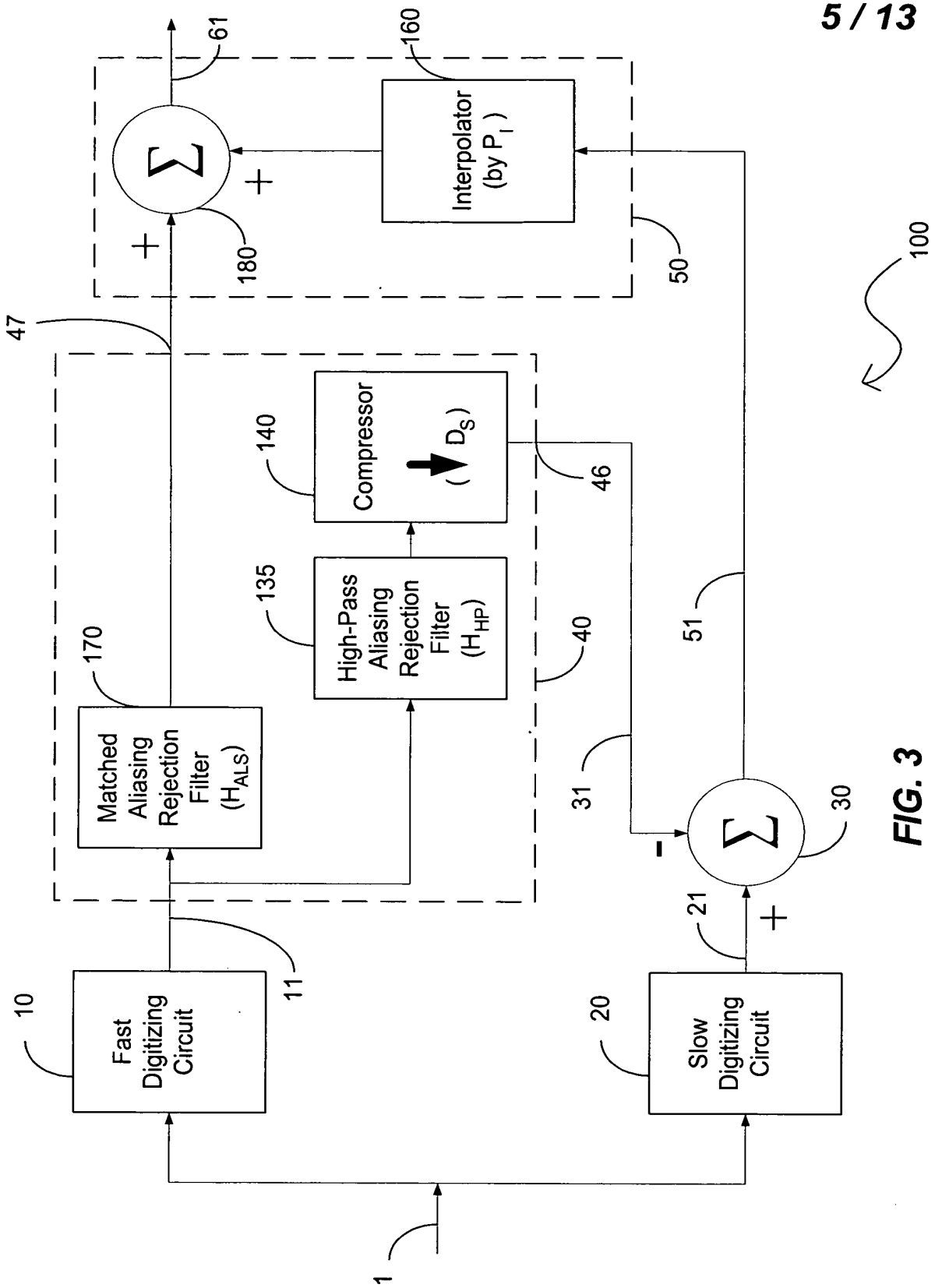
61
160
Interpolator (by P_I)
Σ
+
+
180
50
100
47
Compressor (D_S)
140
46
High-Pass Aliasing Rejection Filter (H_{HP})
135
40
51
Matched Aliasing Rejection Filter (H_{ALS})
170
31
-
Σ
30
21
+
10
Fast Digitizing Circuit
11
20
Slow Digitizing Circuit
1

FIG. 3

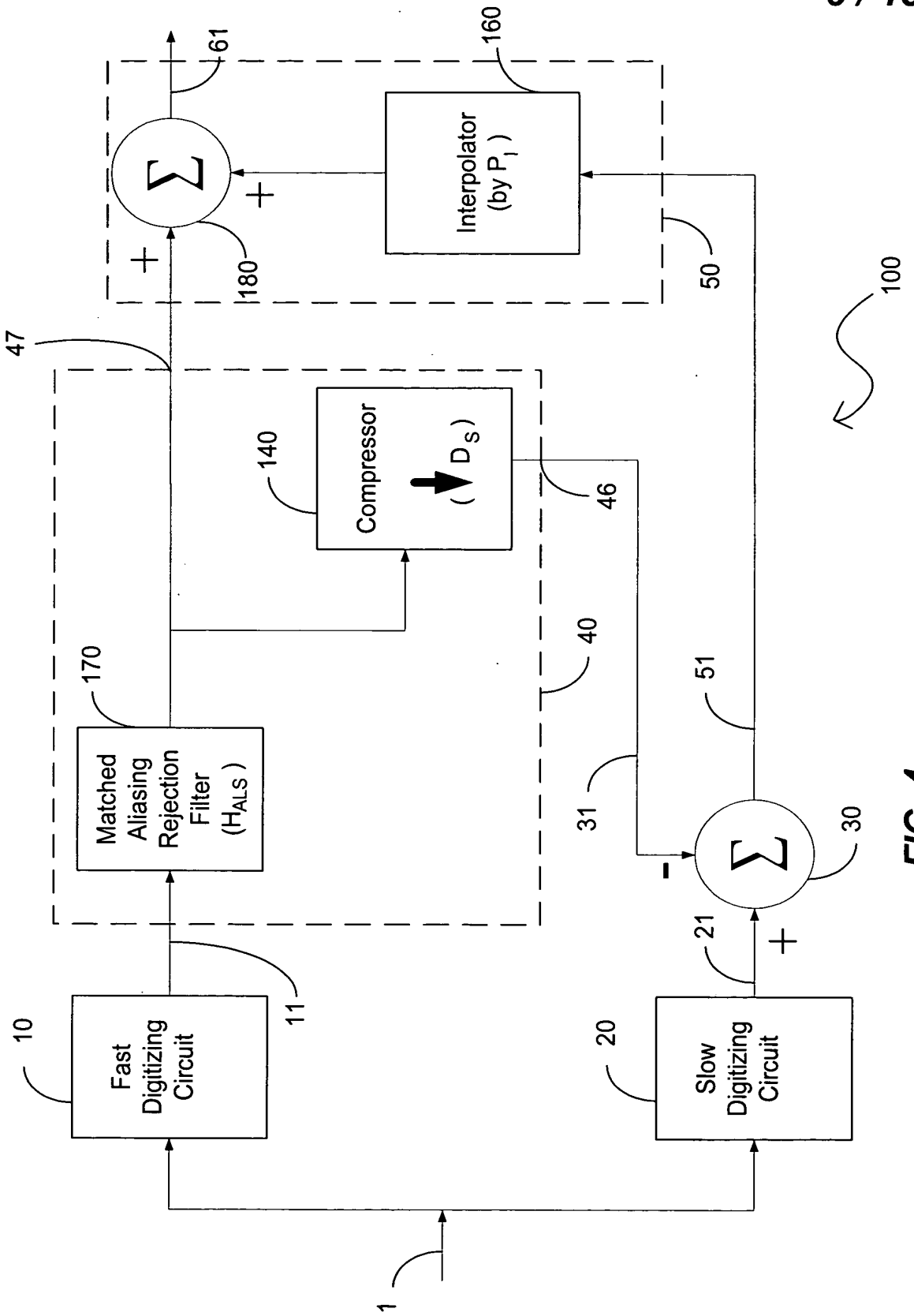
61
160
Σ
Interpolator (by P_I)
+
+
180
50
100
47
140
Compressor (D_S)
46
40
170
51
Matched Aliasing Rejection Filter (H_{ALS})
31
-
Σ
30
21
+
10
Fast Digitizing Circuit
11
20
Slow Digitizing Circuit
1

FIG. 4

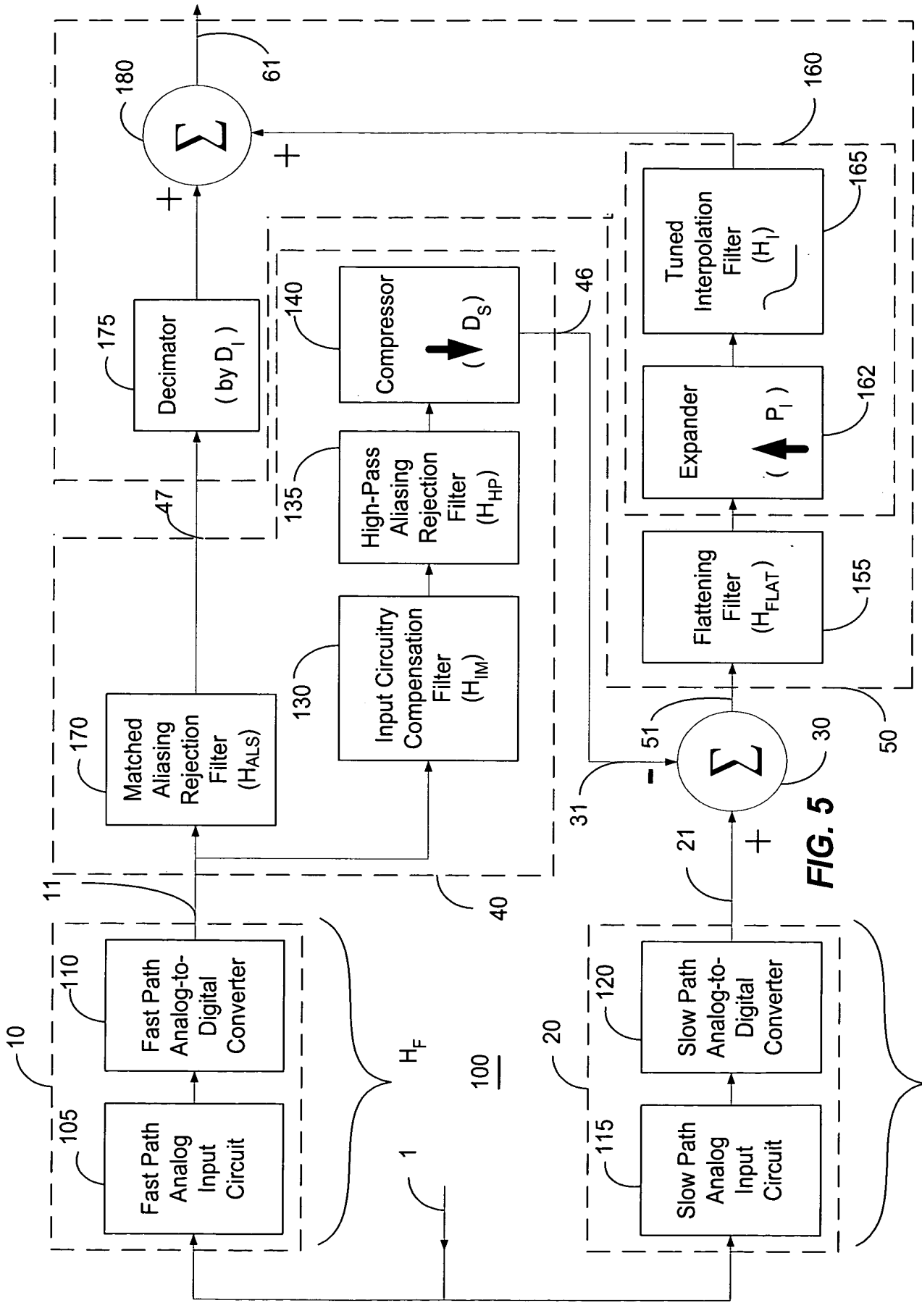
10
Fast Path Analog Input Circuit
105
Fast Path Analog-to-Digital Converter
110
11
H_F
1
100
20
Slow Path Analog Input Circuit
115
Slow Path Analog-to-Digital Converter
120
H_S
40
Matched Aliasing Rejection Filter (H_{ALS})
170
Input Circuitry Compensation Filter (H_{IM})
130
High-Pass Aliasing Rejection Filter (H_{HP})
135
Compressor (D_S)
140
46
47
Decimator (by D_I)
175
180
61
Flattening Filter (H_{FLAT})
155
Expander (P_I)
162
Tuned Interpolation Filter (H_I)
165
160
50
51
30
31
21

FIG. 5

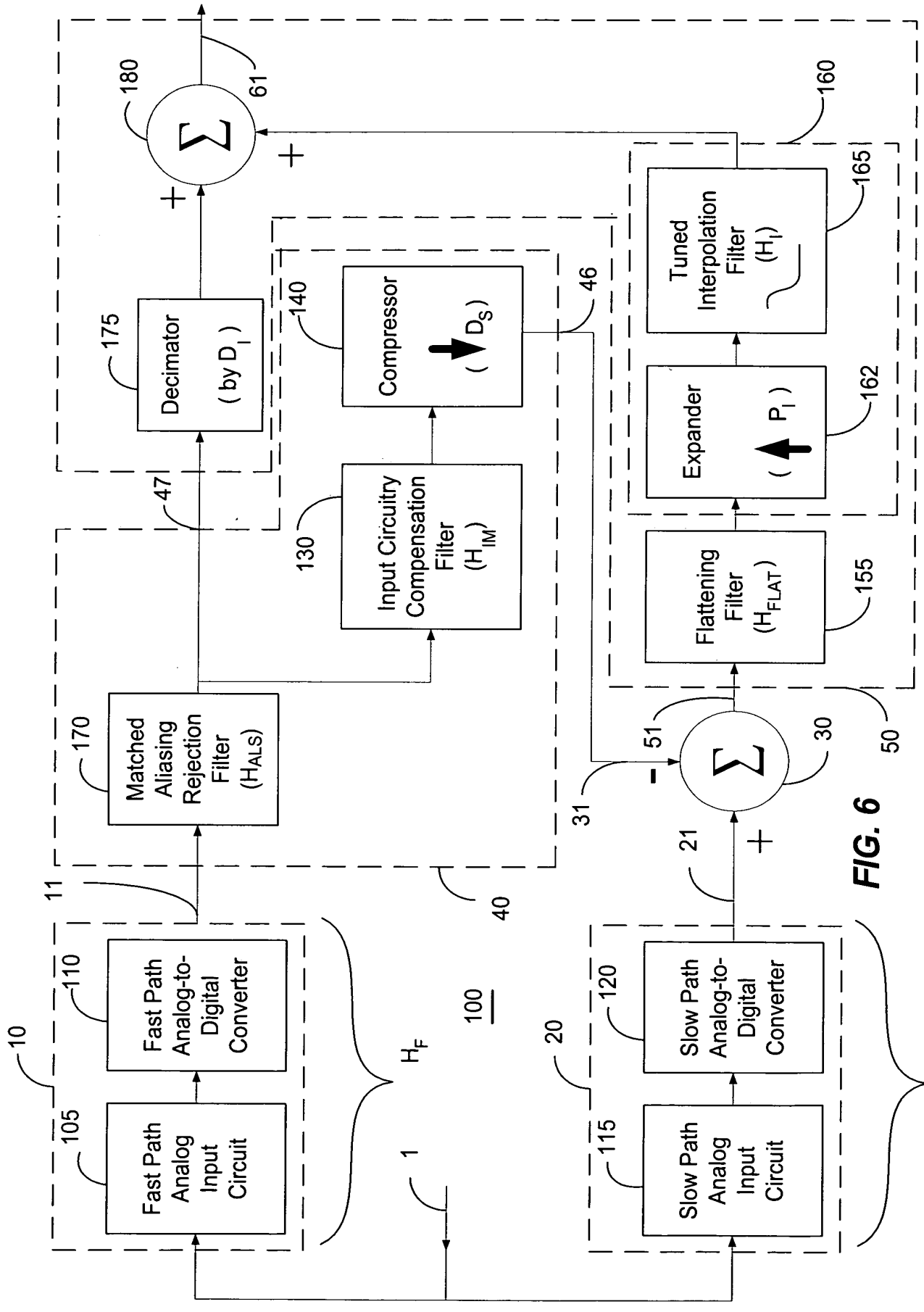
10
105
Fast Path Analog Input Circuit
110
Fast Path Analog-to-Digital Converter
H_F
1
100
20
115
Slow Path Analog Input Circuit
120
Slow Path Analog-to-Digital Converter
H_S
11
40
47
Matched Aliasing Rejection Filter (H_{ALS})
170
Input Circuitry Compensation Filter (H_{IM})
130
Compressor (D_S)
140
Decimator (by D_I)
175
180
61
46
Flattening Filter (H_{FLAT})
155
Expander (P_I)
162
Tuned Interpolation Filter (H_I)
165
160
50
51
30
31
21

FIG. 6

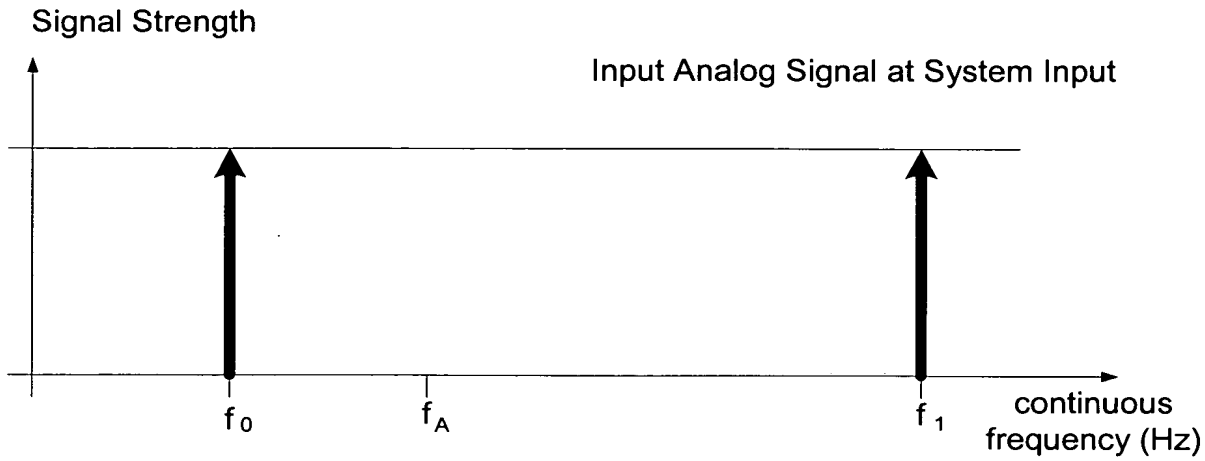

FIG. 7A

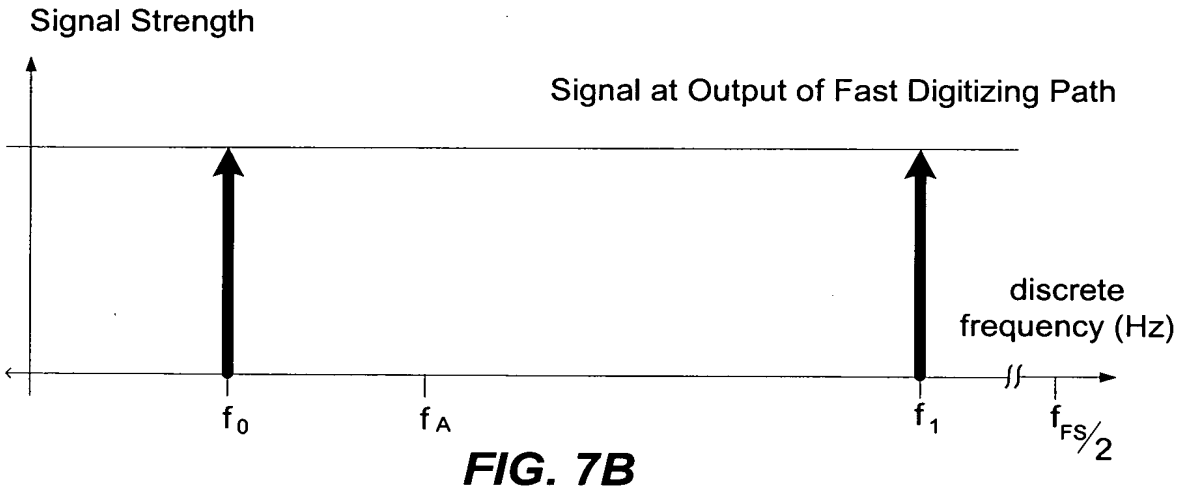

FIG. 7B

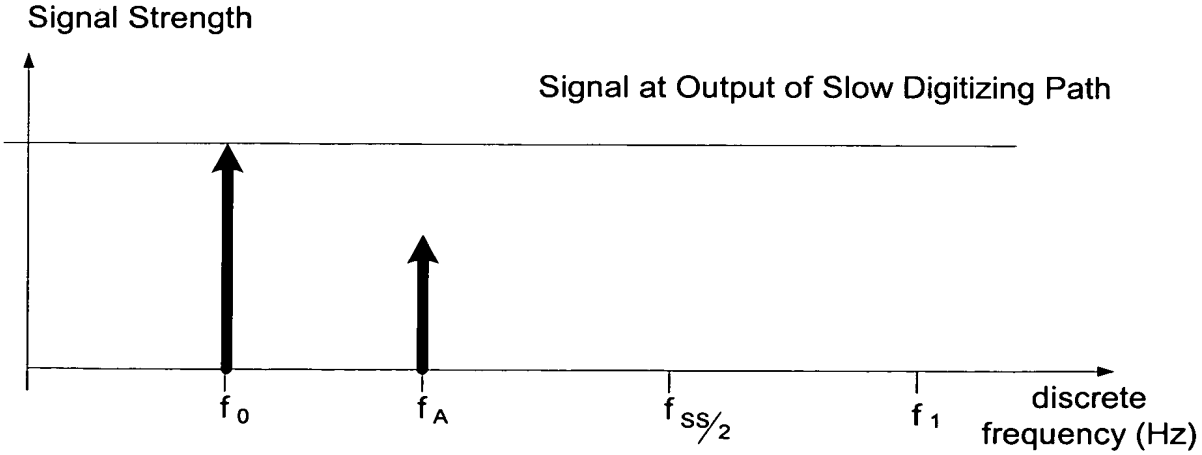

FIG. 7C

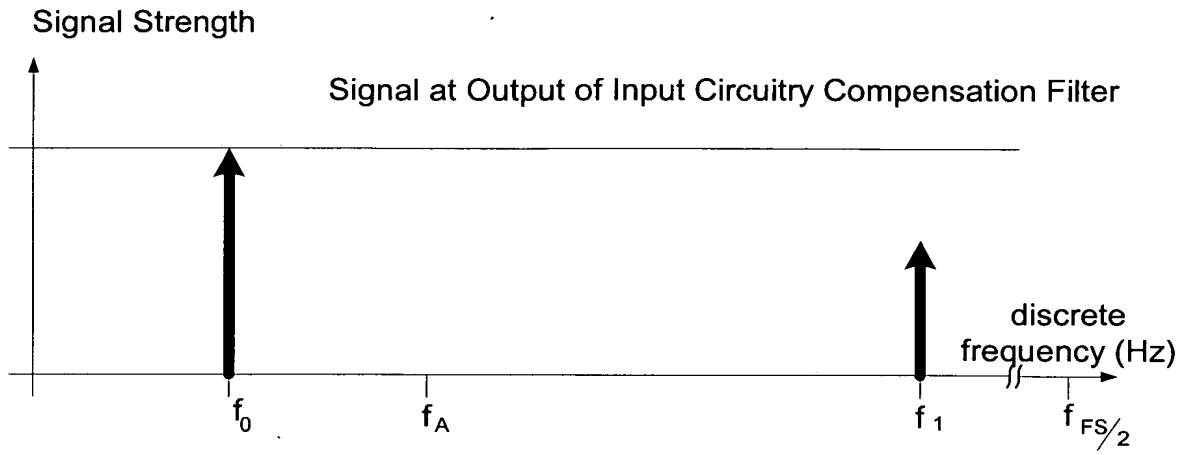

FIG. 7D

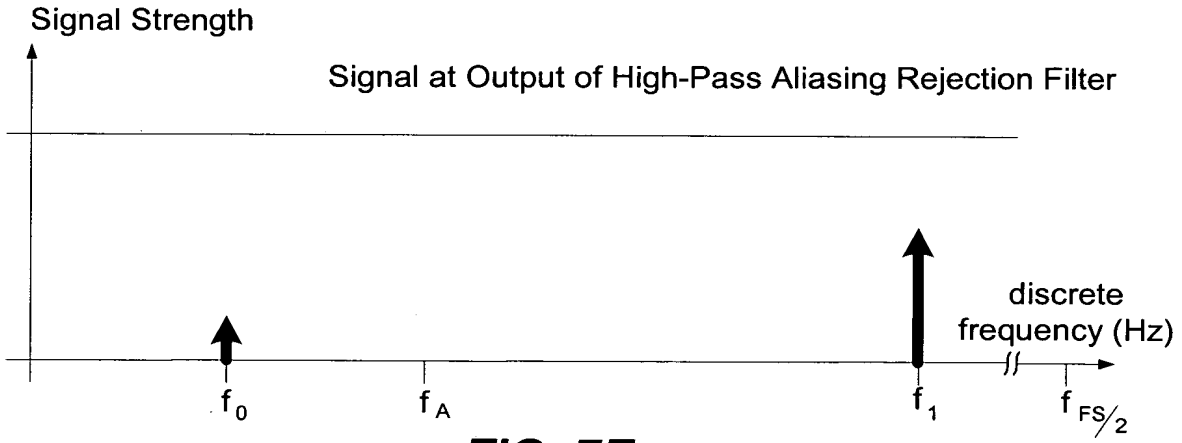

FIG. 7E

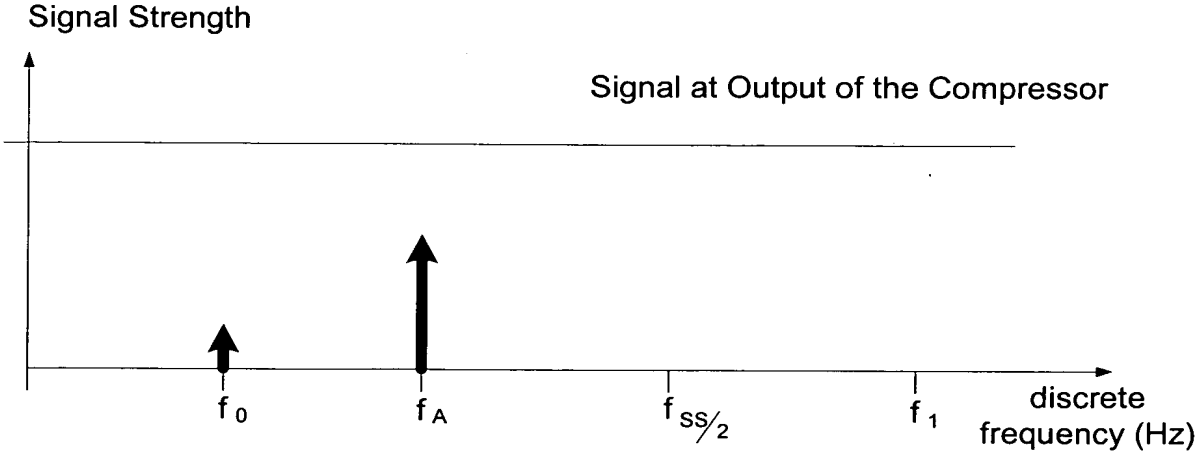

FIG. 7F

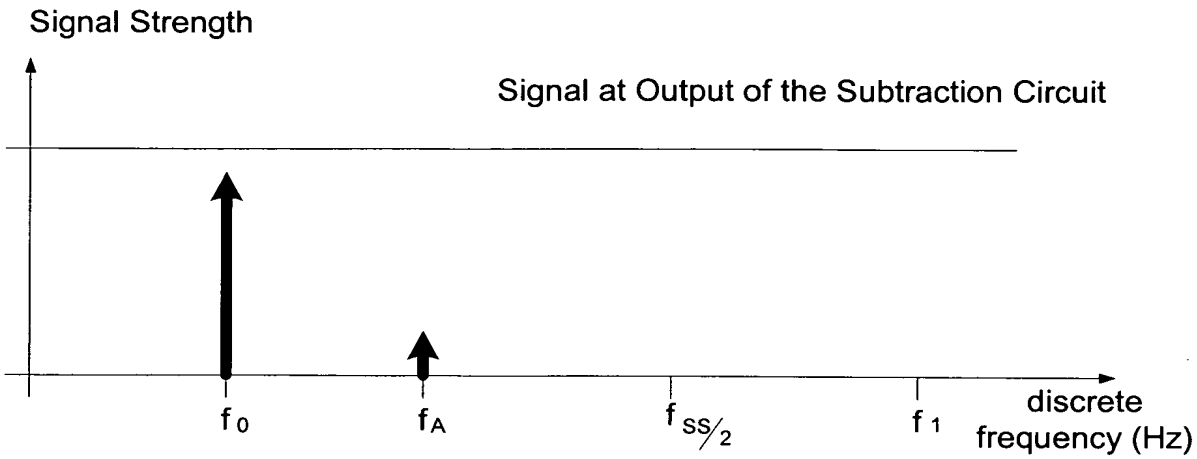

FIG. 7G

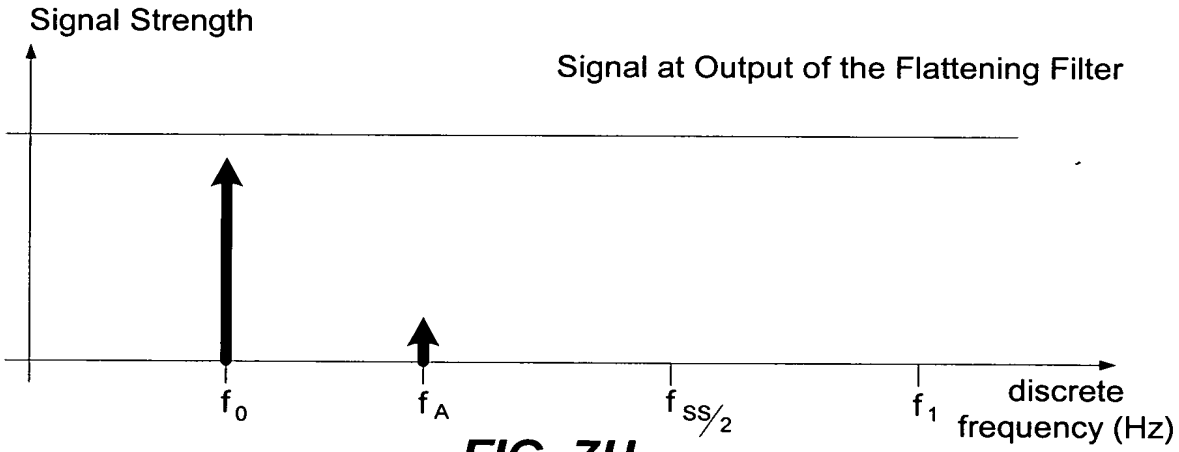

FIG. 7H

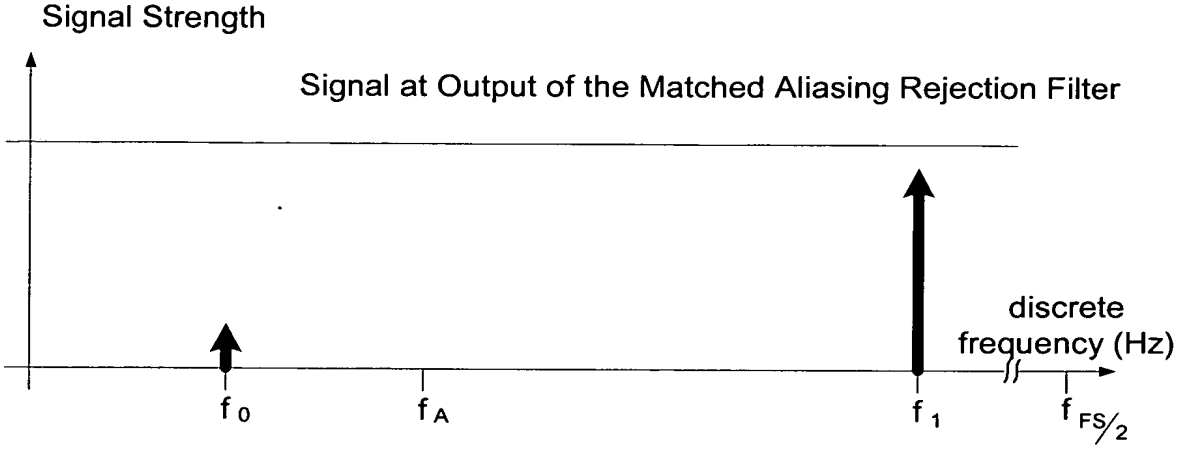

FIG. 7I

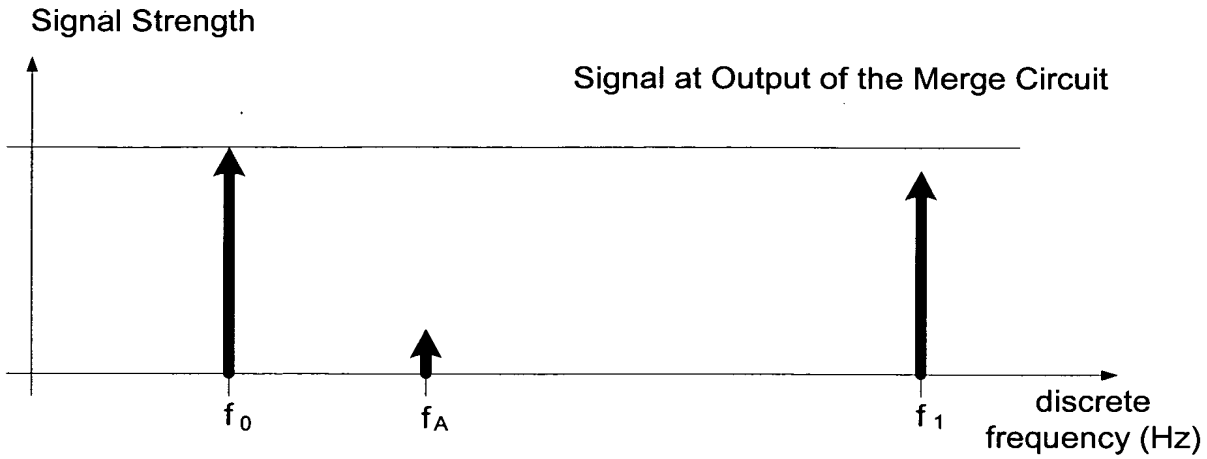
Signal Strength
Signal at Output of the Merge Circuit
f 0
fA
f 1
discrete
frequency (Hz)

FIG. 7J

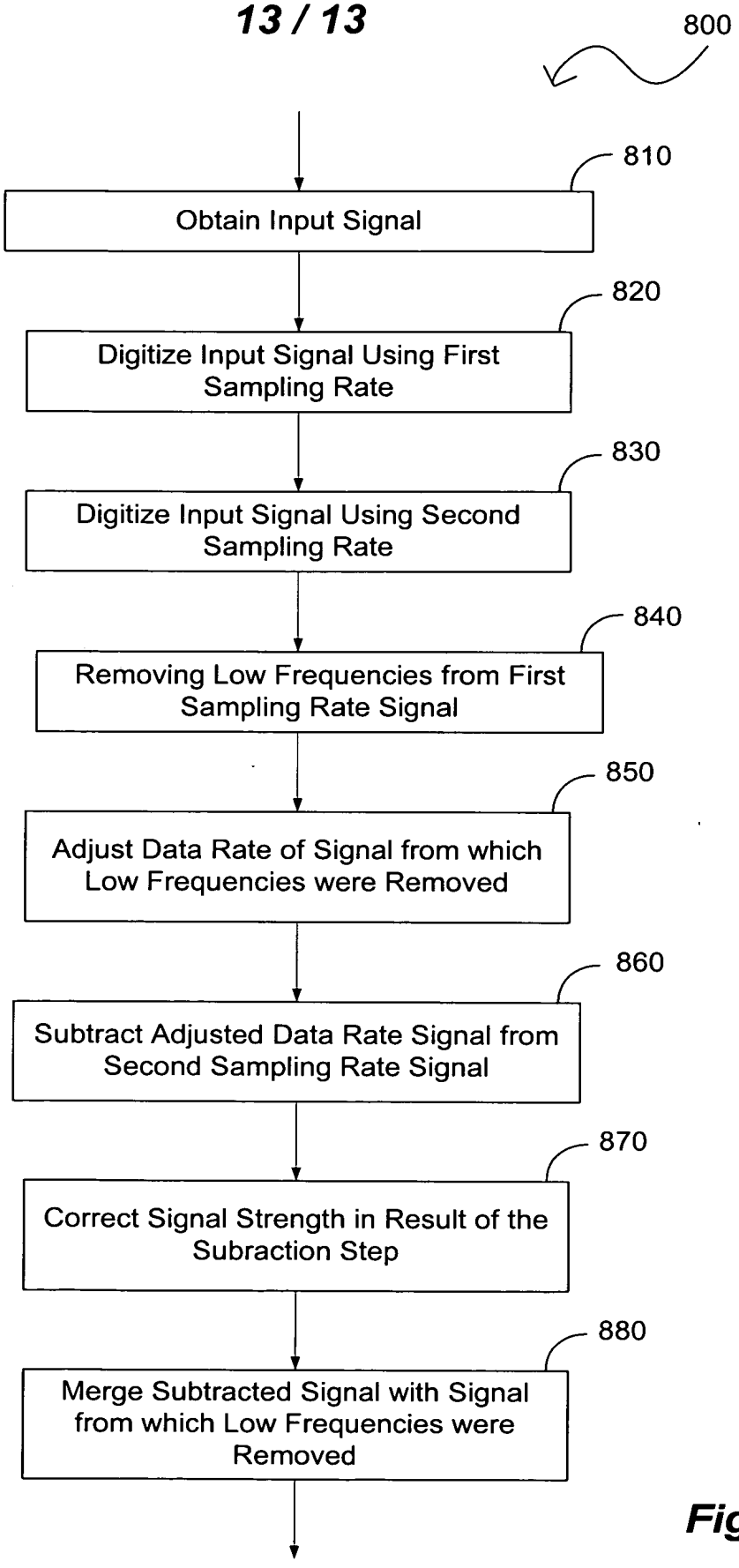
800
810
Obtain Input Signal
820
Digitize Input Signal Using First Sampling Rate
830
Digitize Input Signal Using Second Sampling Rate
840
Removing Low Frequencies from First Sampling Rate Signal
850
Adjust Data Rate of Signal from which Low Frequencies were Removed
860
Subtract Adjusted Data Rate Signal from Second Sampling Rate Signal
870
Correct Signal Strength in Result of the Subraction Step
880
Merge Subtracted Signal with Signal from which Low Frequencies were Removed

Fig. 8